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REMARKS

Claims 1-20 are pending in the present application. By virtue of this response, claims 2, 3, and 10 have been amended. Accordingly, claims 1-20 are currently under consideration. Amendment and cancellation of certain claims are not to be construed as dedication to the public of any of the subject matter previously presented.

Claim Objection

Applicants have amended claims 2 and 10 to address the informalities identified in the Office Action.

Claim Rejection under 35 U.S.C. § 102

Claims 1-5, 8, 13-14, and 16-17 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Ahrikencheikh et al. (U.S. Patent No. 6,334,100, hereinafter the Ahrikencheikh reference). Applicants respectfully traverse these rejections.

In response, Applicants respectfully submit that the Ahrikencheikh reference does not disclose each and every element of the claims of the present invention. In particular, Applicants submit that the Ahrikencheikh reference does not disclose at least the element "checking for correctness of the first set of model results by determining whether the first set of model results interrelate according to a plurality of rules" of the independent claims 1, 13, and 16 of the present invention.

The Ahrikencheikh reference discloses a method for modeling components on a printed circuit board. Figure 5 of the Ahrikencheikh reference discloses a model that includes model element identifier, model element type, nominal model component value, model tolerance, etc (see Ahrikencheikh, column 9:47 – column 10:9.) The model correction computer program determines a minimum list of component(s) which must be specified in order for the model correction computer program to compute the remaining values of the elements of the model. The method determines the

types and values of the components of the model when a minimum set of other components are specified as known. (See Ahrikencheikh, column 8:57-65.)

On the contrary, the present invention is distinguished from the Ahrikencheikh reference because it uses a model derived from the SPICE (Simulation Program with Integrated Circuit Emphasis) model developed at the University of California, Berkeley. For example, the present invention models charges (Q), conductance matrix (G), and capacitance matrix (C) for representing an integrated circuit. For non-linear circuits, such as a transistor, the SPICE model solves such circuit equations using the Newton-Ralphson (N-R) iteration. (See page 2 of the present application.)

In addition, Applicants respectfully submit that the Ahrikencheikh reference is silent about the claim limitation "determining whether the first set of model results interrelate according to a plurality of rules." The Applicants cannot find this element of the independent claims disclosed anywhere in the Ahrikencheikh reference. In the present invention. Applicants have taught ten rules for determining the set of model results interrelate to each other according to embodiments of the present invention. (See page 9, paragraph [0027].)

Therefore, for at least the reasons presented above, Applicants assert that claims 1, 13 and 16 are allowable over the Ahrikencheikh reference. Applicants also assert that claims 2-12, 14-15, and 17-20, which variously depend from independent claims 1, 13, and 16, are allowable for at least the reason that they depend from an allowable independent claim.

With respect to claims 2, Applicants respectfully submit that the Ahrikencheikh reference does not disclose at least the elements "determining whether the model results interrelate according to the plurality of rules comprises determining whether the sum of the plurality of entries in the current vector is zero" of the present invention. The Office Action identifies the Simplified Tableau Model allegedly discloses this claim element. Upon a close review of the Simplified Tableau Model, Applicants note that the Ahrikencheikh is silent about this claim element. Instead, the Ahrikencheikh reference states that "[I]if a branch is described by its impedance K_i, the corresponding value of K_y should be set equal to one; and vice versa." "Thus, all K^i_{ij} are zero except

for those diagonal elements K^{i}_{ii} which are set equal to one." Example values of the matrix discussed above are given in Equation 22 of the Ahrikencheikh reference, where a method is derived to use the elements of the reduced matrix Z_m along with information on known components to obtain the types and values of the unknown components of the circuit.

$$\begin{bmatrix} K_i & -K_v A^T \\ A & 0 \end{bmatrix} \begin{bmatrix} N & P \\ Z & Q \end{bmatrix} = \begin{bmatrix} 1 & 0 & \dots & 0 & 0 \\ 0 & 1 & 0 & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & \dots & 0 & 1 & 0 \\ 0 & 0 & \dots & 0 & 1 \end{bmatrix} = 1_{(b-n)\times(b+n)} \qquad \text{(Eq. 22)}$$

As shown in Equation 22 (see Ahrikencheikh, column 14:30), the matrix has value 1 along its diagonal and has value 0 elsewhere. Applicants respectfully submit that it is impossible for the sum of the plurality of entries of this matrix to be zero. Therefore, for at least this reason, Applicants assert that claim 2 is allowable over the Ahrikencheikh reference.

With respect to claims 3, for the similar reasons presented in claim 2, Applicants respectfully submit that the Ahrikencheikh reference fails to disclose the sum of the plurality of entries of the charge vector is zero.

With respect to claims 4, for the similar reasons presented in claim 2, Applicants respectfully submit that the Ahrikencheikh reference fails to disclose the sum of the entries in each of the plurality of rows of entries is zero.

With respect to claims 5, for the similar reasons presented in claim 2, Applicants respectfully submit that the Ahrikencheikh reference fails to disclose the sum of the entries in each of the plurality of columns of entries is zero.

Claim Rejection under 35 U.S.C. § 103

Claims 6-7, 9-10, and 18 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Ahrikencheikh et al. in view of Nguyen et al. (1998), "Simulation of Coupling Capacitances Using Matrix Partitioning", International Conference on Computer-Aided Design

(ICCD 1988), Proceedings of the 1998 IEEE/ACM International Conference on Computer-Aided Design, San Jose, California, US, pages 12-18 (hereinafter the Nguyen reference). Claims 11-12, 15, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahrikencheikh etal. in view of Sharrit (U.S. Patent No. 5,588,142).

With respect to claim 6, the Office Action identifies section 2 of the Nguyen reference allegedly discloses this claim element. Upon a close review of the Nguyen reference, Applicants respectfully submit that it is silent about the claim element of "wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether the sum of the entries in each of the plurality of rows of entries is zero."

In addition, Applicants respectfully submit that claims 6-7, 9-12, 15, and 18-20 are allowable for at least the reason that they depend from an allowable independent claim.

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CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 188122000700. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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